IN THE CLAIMS

1. (Currently amended) An integrated circuit comprising:

a voltage controlled oscillator (VCO) operative to provide an oscillator signal having a frequency; ~~and~~

at least one reverse biased diode having a capacitance that is controlled by a reverse bias voltage to compensate for drift in the frequency of the oscillator signal due to temperature;

a bias voltage generator to provide the reverse bias voltage for the at least one reverse biased diode, the bias voltage generator including a circuit component having a characteristic that is proportional to absolute temperature (PTAT), and wherein the reverse bias voltage is generated based on the PTAT characteristic of the circuit component.

2. (Original) The integrated circuit of claim 1, wherein each of the at least one reverse biased diode is formed by a parasitic diode in the integrated circuit.

3. (Original) The integrated circuit of claim 2, wherein the parasitic diode is formed at a drain junction or a source junction of a metal-oxide semiconductor (MOS) transistor.

4. (Original) The integrated circuit of claim 1, wherein the VCO includes

an amplifier operative to provide signal gain for the VCO,

a resonator tank circuit operative to provide phase shift for the VCO, and

at least one frequency tuning circuit operative to tune the frequency of the oscillator signal, each frequency tuning circuit including at least one tuning capacitor and at least one metal-oxide semiconductor (MOS) transistor operative to connect or disconnect the at least one tuning capacitor from the resonator tank circuit.

5. (Original) The integrated circuit of claim 4, wherein the VCO includes a plurality of frequency tuning circuits having progressively larger tuning capacitors.

6. (Original) The integrated circuit of claim 5, wherein for each of the plurality of frequency tuning circuits, the at least one MOS transistor for the frequency tuning circuit is sized proportional to capacitance of the at least one tuning capacitor for the frequency tuning circuit.

7. (Original) The integrated circuit of claim 4, wherein the at least one reverse biased diode is formed by parasitic diode at the at least one MOS transistor.

8. Canceled

9. Canceled

10. (Original) The integrated circuit of claim ~~9~~ 1, wherein the circuit component is a current source providing a bias current that is proportional to absolute temperature.

11. (Original) The integrated circuit of claim ~~9~~ 1, wherein the circuit component is a resistor having a resistance that is proportional to absolute temperature.

12. (Currently amended) ~~The integrated circuit of claim 8, wherein the bias voltage generator includes~~ An integrated circuit comprising:

a voltage controlled oscillator (VCO) operative to provide an oscillator signal having a frequency;

at least one reverse biased diode having a capacitance that is controlled by a reverse bias voltage to compensate for drift in the frequency of the oscillator signal due to temperature;

a current source operative to provide a bias current;

a current mirror operative to provide at least one version of the bias current; and

a load resistor operative to receive the at least one version of the bias current and provide the reverse bias voltage.

13. (Original) The integrated circuit of claim 12, wherein the at least one version of the bias current is selectable from among a plurality of possible versions of the bias

current, and wherein different functions of reverse bias voltage versus temperature are obtained by selecting different combinations of bias current versions.

14. (Currently amended) The integrated circuit of claim ~~8~~ 1, wherein the bias voltage generator includes:

a look-up table operative to store a function of reverse bias voltage versus temperature, and

a digital-to-analog converter operative to receive a temperature dependent value from the look-up table and provide the reverse bias voltage.

15. (Original) The integrated circuit of claim 1, wherein the oscillator signal is a local oscillator (LO) signal that is suitable for frequency upconversion or downconversion in a wireless communication system.

16. (Original) The integrated circuit of claim 15, wherein the wireless communication system is a Code Division Multiple Access (CDMA) system.

17. (Original) The integrated circuit of claim 15, wherein the wireless communication system is a Global System for Mobile Communications (GSM) system.

18. A wireless device comprising:

a voltage controlled oscillator (VCO) operative to provide an oscillator signal having a frequency; ~~and~~

at least one reverse biased diode having a capacitance that is controlled by a reverse bias voltage to compensate for drift in the frequency of the oscillator signal due to temperature; and

a bias voltage generator operative to provide the reverse bias voltage for the at least one reverse biased diode, the bias voltage generator including a circuit component having a characteristic that is proportional to absolute temperature (PTAT), and the reverse bias voltage being generated based on the PTAT characteristic of the circuit component.

19. (Original) The wireless device of claim 18, wherein each of the at least one reverse biased diode is formed by a parasitic diode at a drain junction or a source junction of a metal-oxide semiconductor (MOS) transistor.

20. Canceled

21. (Currently amended) An apparatus comprising:

a voltage controlled oscillator (VCO) operative to provide an oscillator signal having a frequency; ~~and~~

at least one reverse biased diode having a capacitance that is controlled by a reverse bias voltage to compensate for drift in the frequency of the oscillator signal due to temperature; and

a bias voltage generator to provide the reverse bias voltage for the at least one reverse biased diode, the bias voltage generator including a circuit component to estimate the temperature of the VCO, and wherein the reverse bias voltage is generated based on the estimated temperature.

22. (Original) The apparatus of claim 21, wherein each of the at least one reverse biased diode is formed by a parasitic diode at a drain junction or a source junction of a metal-oxide semiconductor (MOS) transistor.

23. Canceled

24. (Currently amended) The method of claim ~~23~~ 25, wherein capacitance of the at least one reverse biased diode is adjusted by the reverse bias voltage to compensate for changes in capacitance of the VCO due to temperature.

25. (Currently amended) ~~The method of claim 23,~~ A method of performing temperature compensation for a voltage controlled oscillator (VCO), comprising:

estimating temperature of the VCO; wherein the temperature of the VCO is estimated with a circuit component having a characteristic that is proportional to absolute temperature

generating a reverse bias voltage for the estimated temperature; and

applying the reverse bias voltage to at least one reverse biased diode to compensate for drift in frequency of oscillation for the VCO due to temperature.

26. (Currently amended) ~~The method of claim 23,~~ A method of performing temperature compensation for a voltage controlled oscillator (VCO), comprising:

estimating temperature of the VCO;

generating a reverse bias voltage for the estimated temperature; and

applying the reverse bias voltage to at least one reverse biased diode to compensate for drift in frequency of oscillation for the VCO due to temperature, wherein the reverse bias voltage is generated based on a selectable function of reverse bias voltage versus temperature.